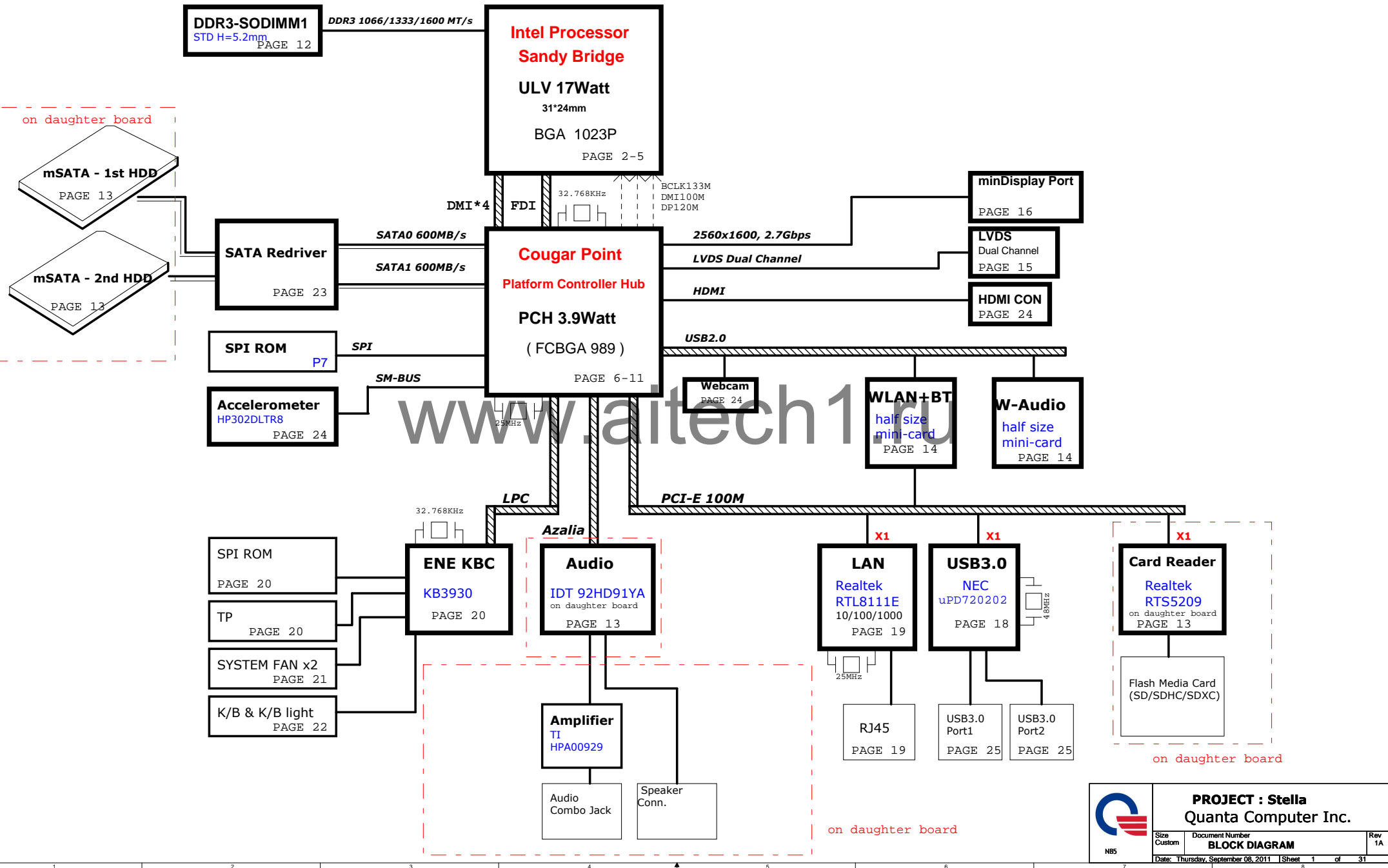
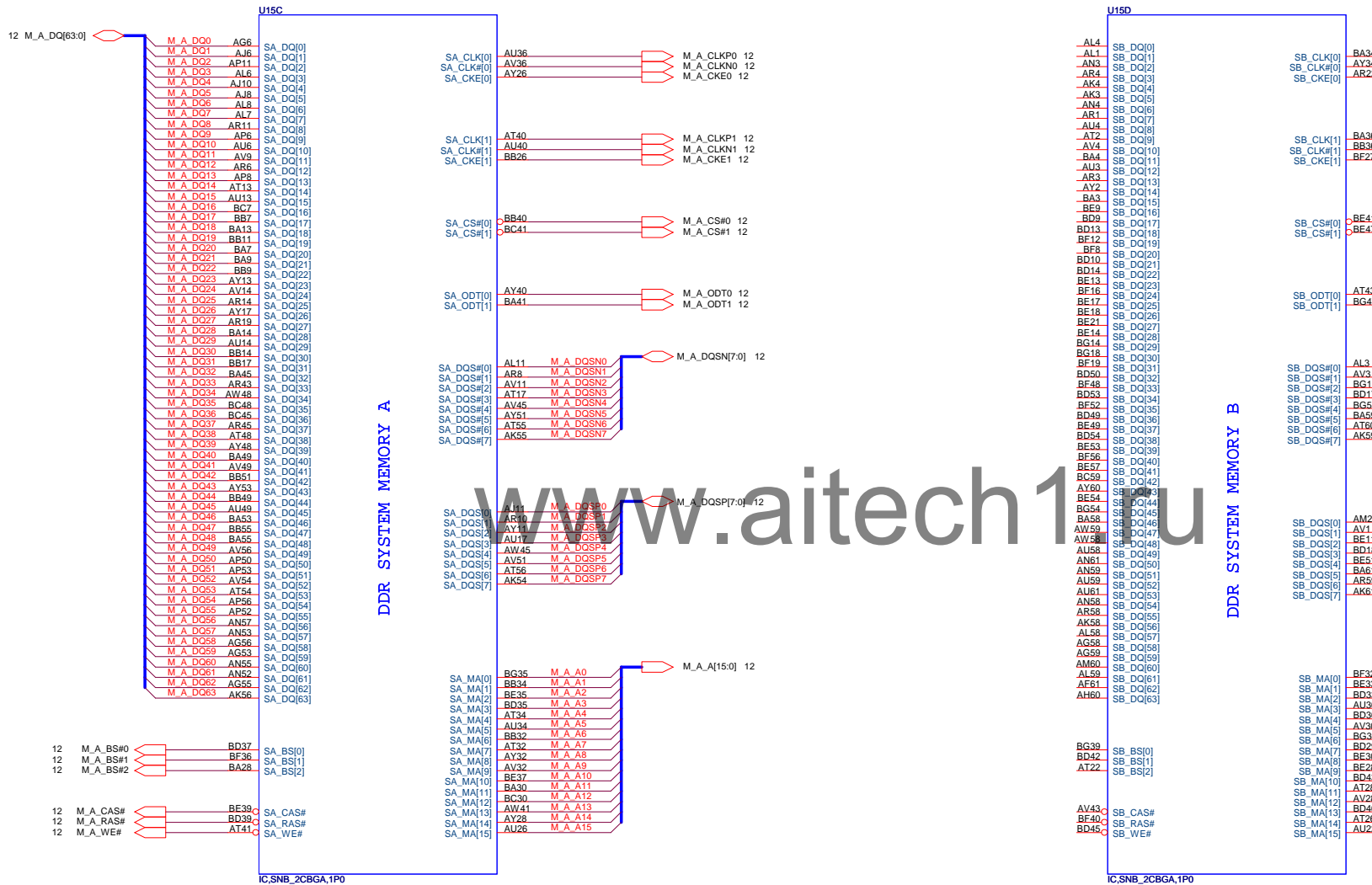


01



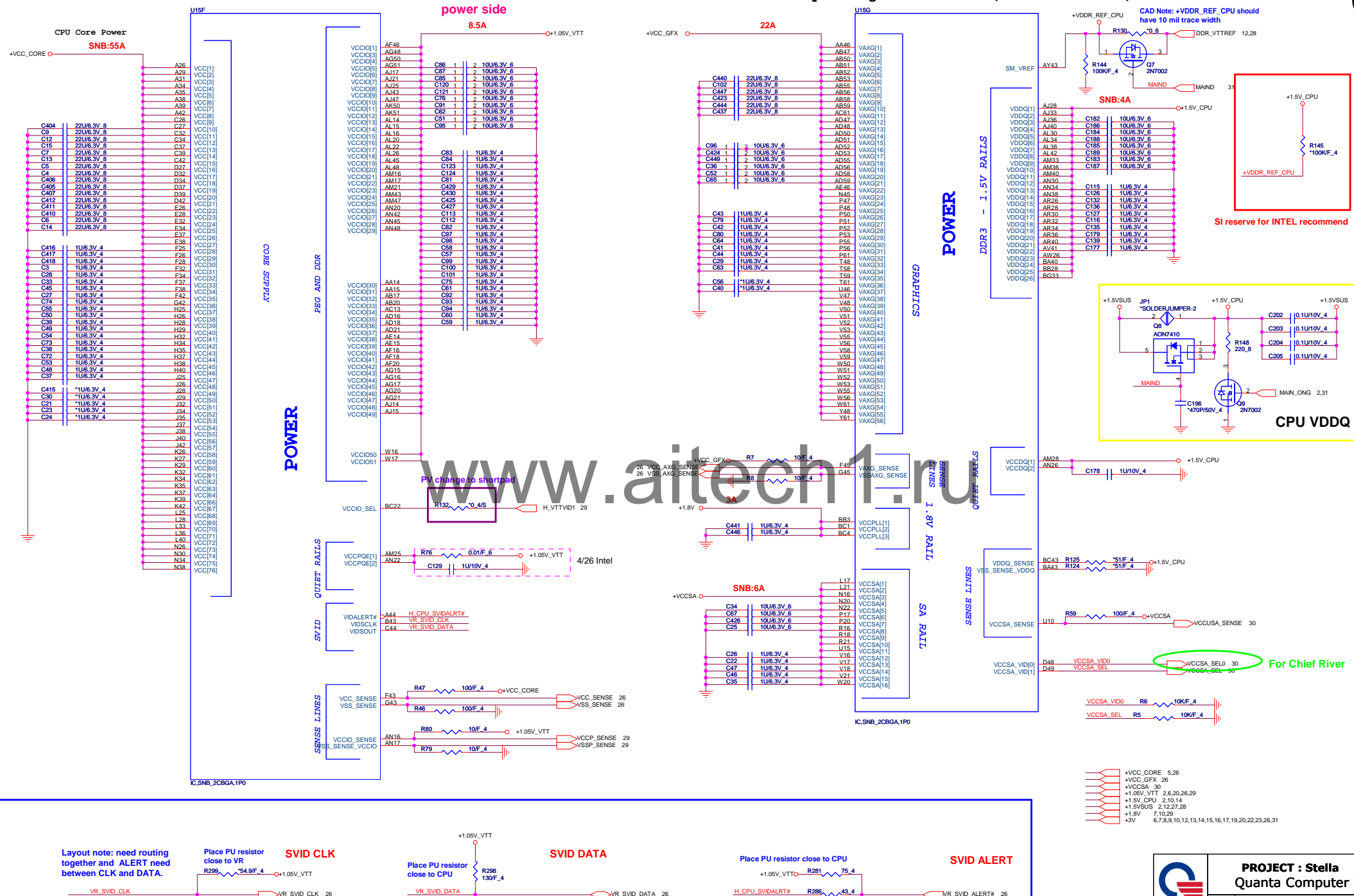
Sandy Bridge Processor (DDR3)



Sandy Bridge Processor (POWER)

330uF locate
power side

Sandy Bridge Processor (GRAPHIC POWER)



Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

SVID CLK

R299 *54.9/F₄

+1.05V VTT

SVID DATA

Place PU resistor close to CPU **SVID ALERT**

+1.05V_VTTO

R281 75.4

H_CPU_SVIDALRT#

R286 43.4

VR_SVID_ALERT# 26

SVID ALERT

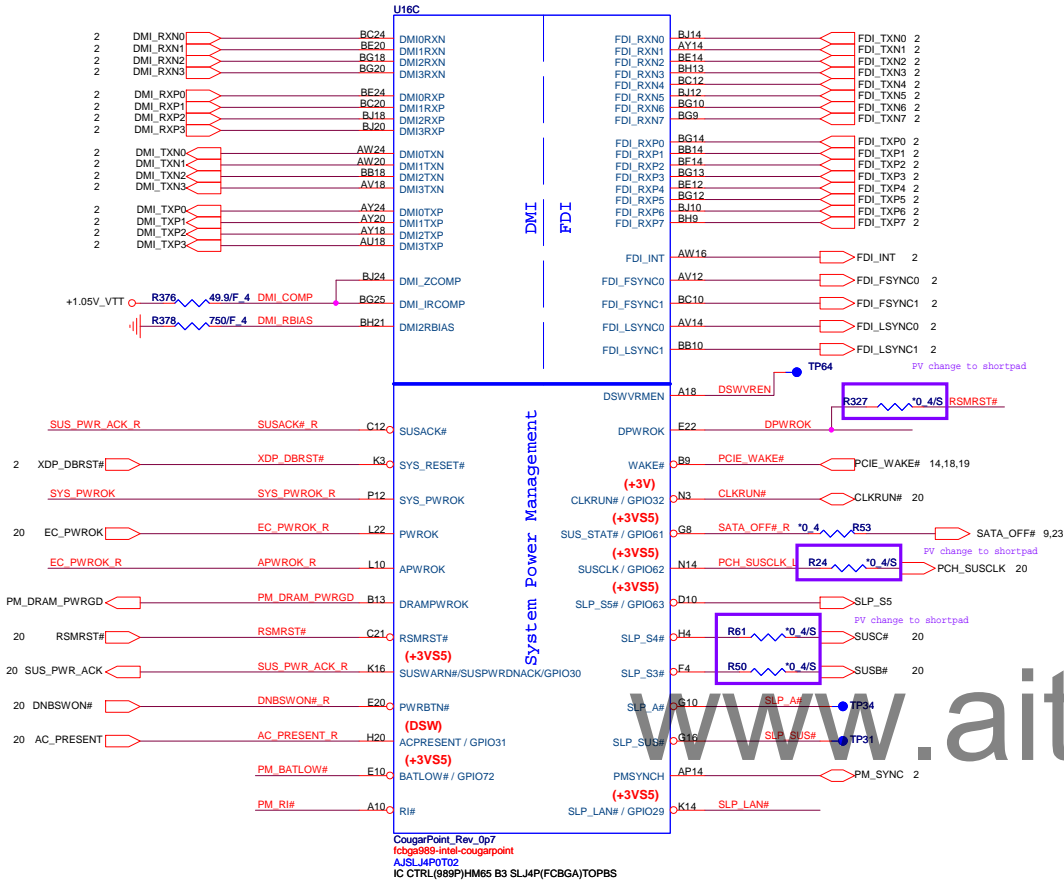


PROJECT : Stella
Quanta Computer Inc.

Size Custom	Document Number SNB 3/4 (POWER)
Date: Friday, September 09, 2011	Sheet 4 of 31

Cougar Point (DMI,FDI,PM)

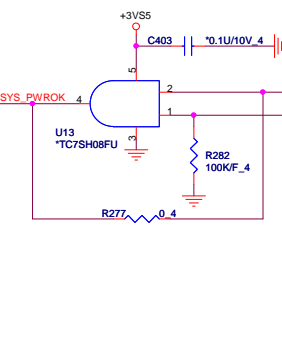
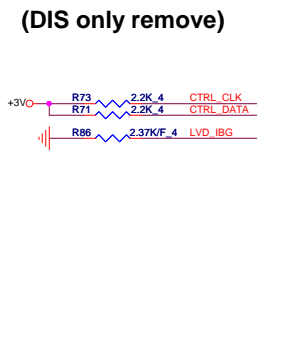
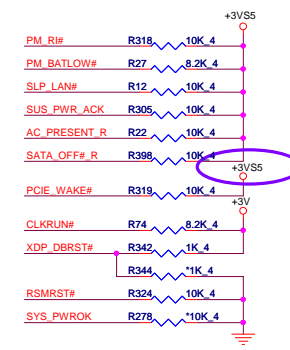
Cougar Point (LVDS,DDI)



PCH Pull-high/low(CLG)

INT LVDS & CRT disable
(DIS only remove)

System PWR_OK(CLG)



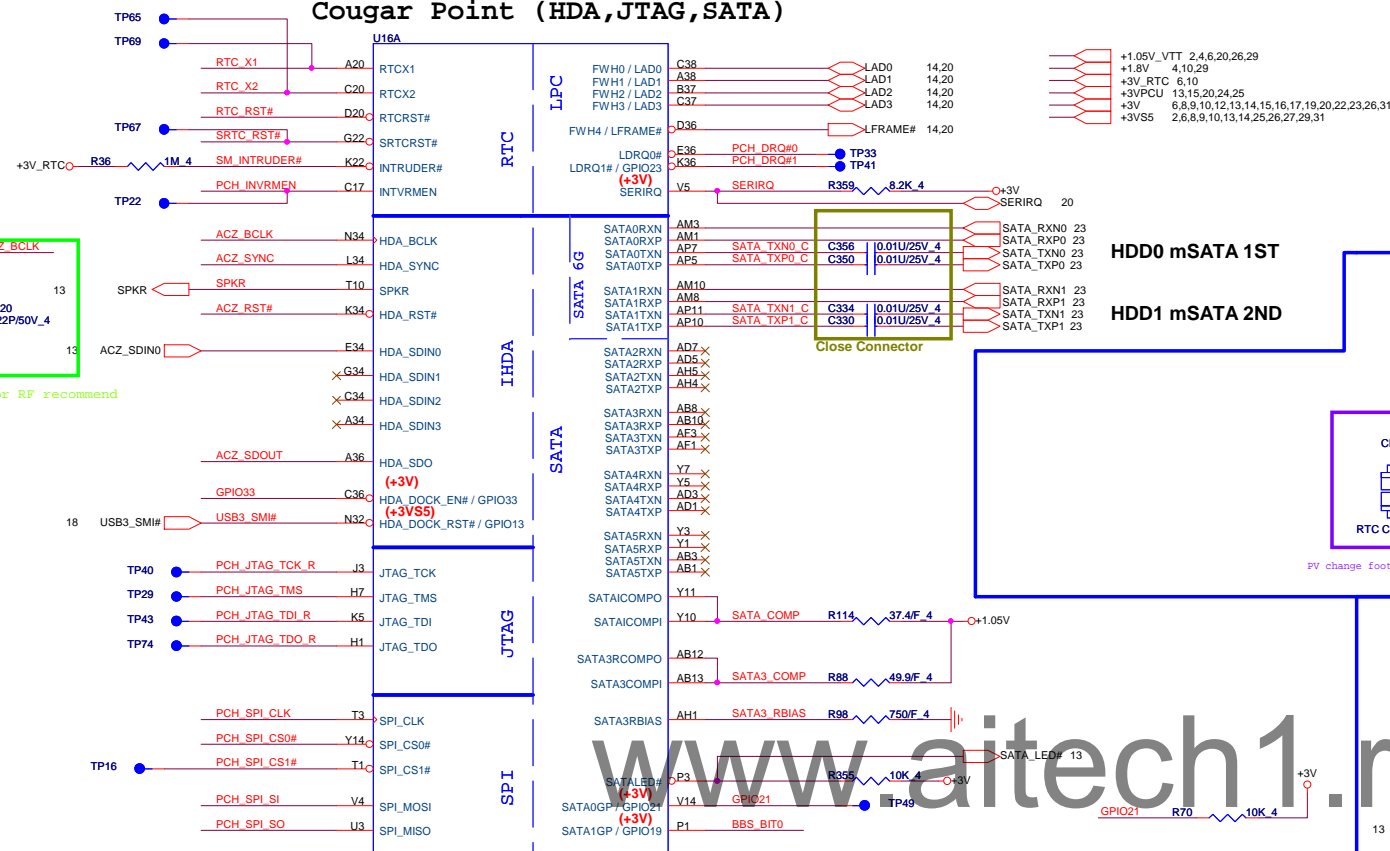
+1.05V_VTT 2,4,20,26,29
+3V_RTC 7,10
+3VS5 2,7,8,9,10,13,14,25,26,27,29,31
+3V 7,8,9,10,12,13,14,15,16,17,19,20,22,23,26,31
+5V 7,10,13,14,15,16,17,21,22,31



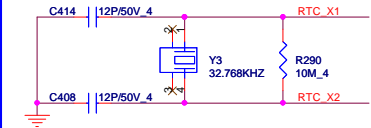
PROJECT : Stella
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Thursday, September 08, 2011	Sheet 6 of 31	

Cougar Point (HDA,JTAG,SATA)



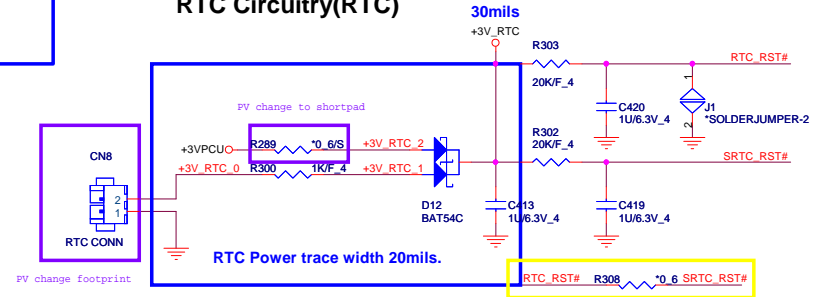
RTC Clock 32.768KHz



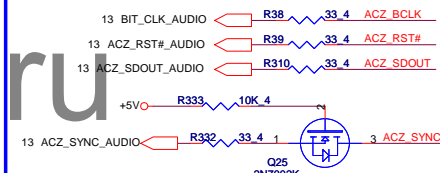
HDD0 mSATA 1ST

HDD1 mSATA 2ND

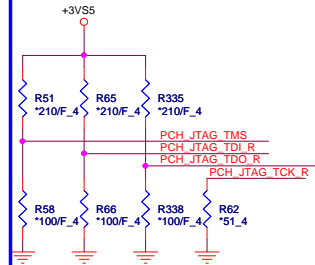
RTC Circuitry(RTC)



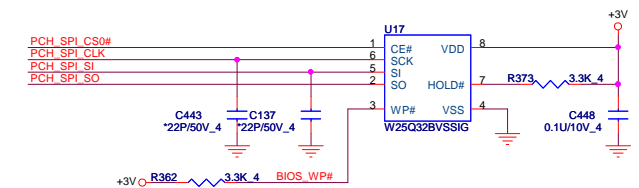
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

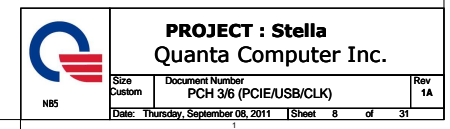


Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PROJECT : Stella Quanta Computer Inc.		
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1A
Date: Friday, September 09, 2011 Sheet 7 of 31		

PCH Strap Table

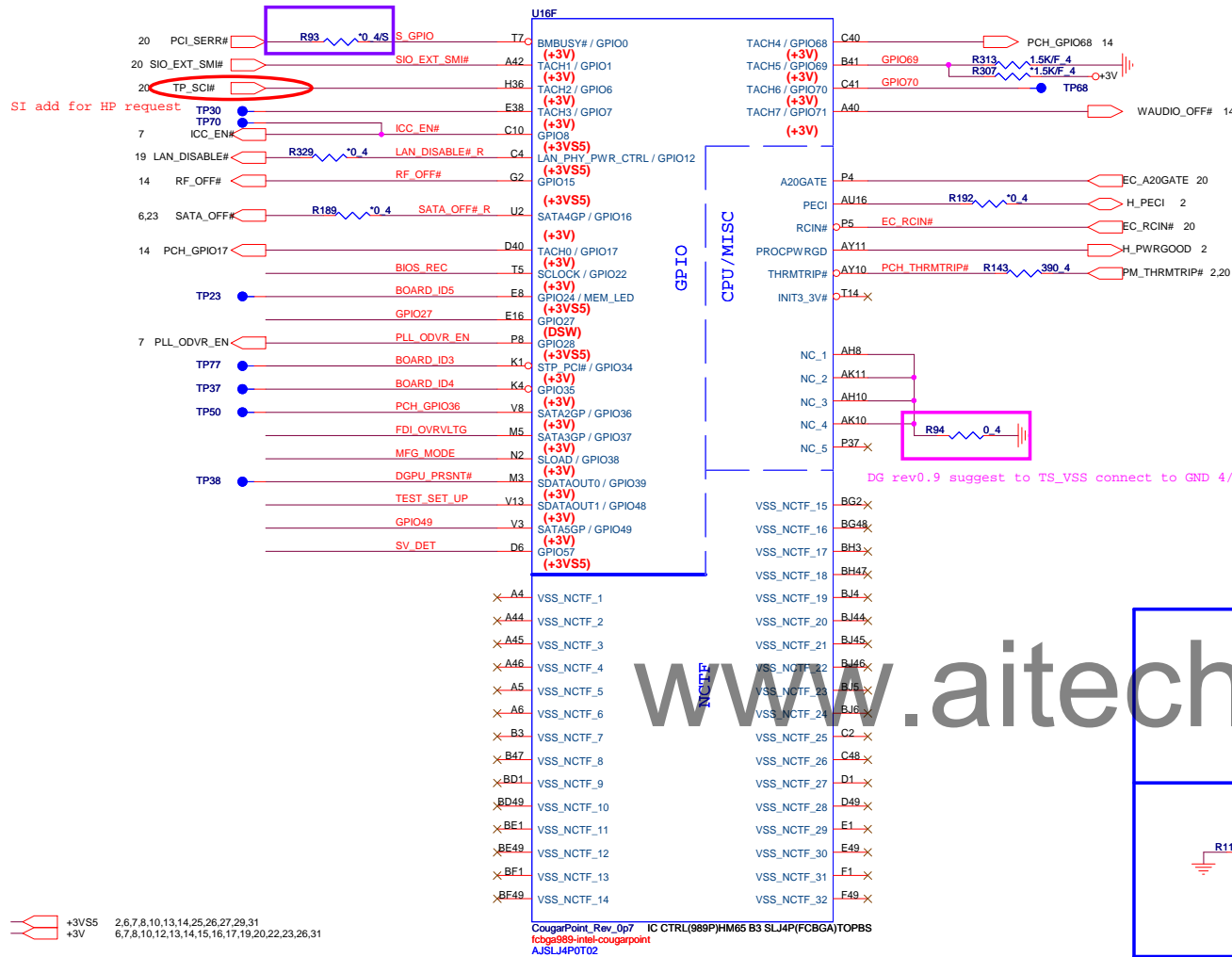
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R87 1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R31 1K_4 R30 10K_4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R41 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R326 1K/F_4 GPIO33_E 20
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R353 1K_4 R339 1K_4 BBS_BIT0 8
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R119 1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R117 2.2K_4 R118 4.7K_4 NV_CLE 8 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R29 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	20 GPIO33_E ACZ_SDO R325 1K_4 +3VS5
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R317 1K_4 ICC_EN# 9
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R82 1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R90 1K/F_4 +3V



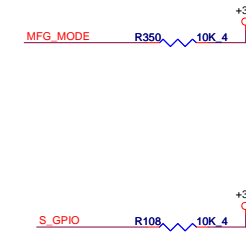
Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

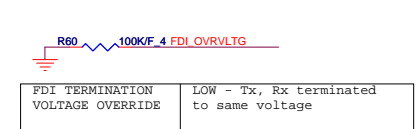
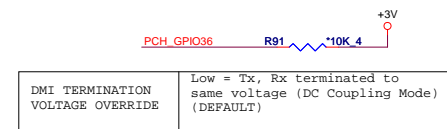
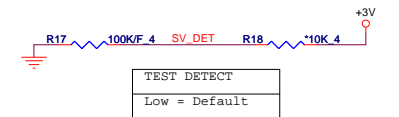
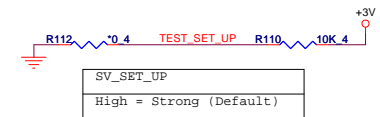
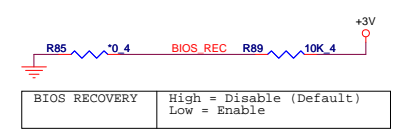
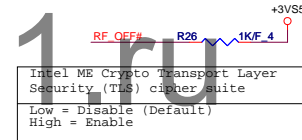
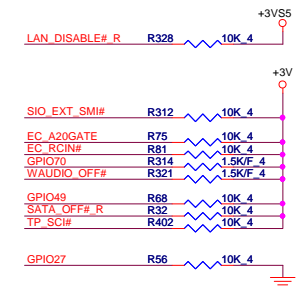
PV change to shortpad



MFG-TEST



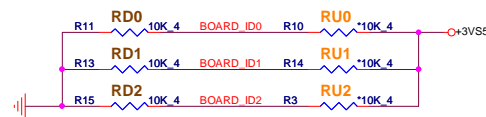
GPIO Pull-up/Pull-down(CLG)



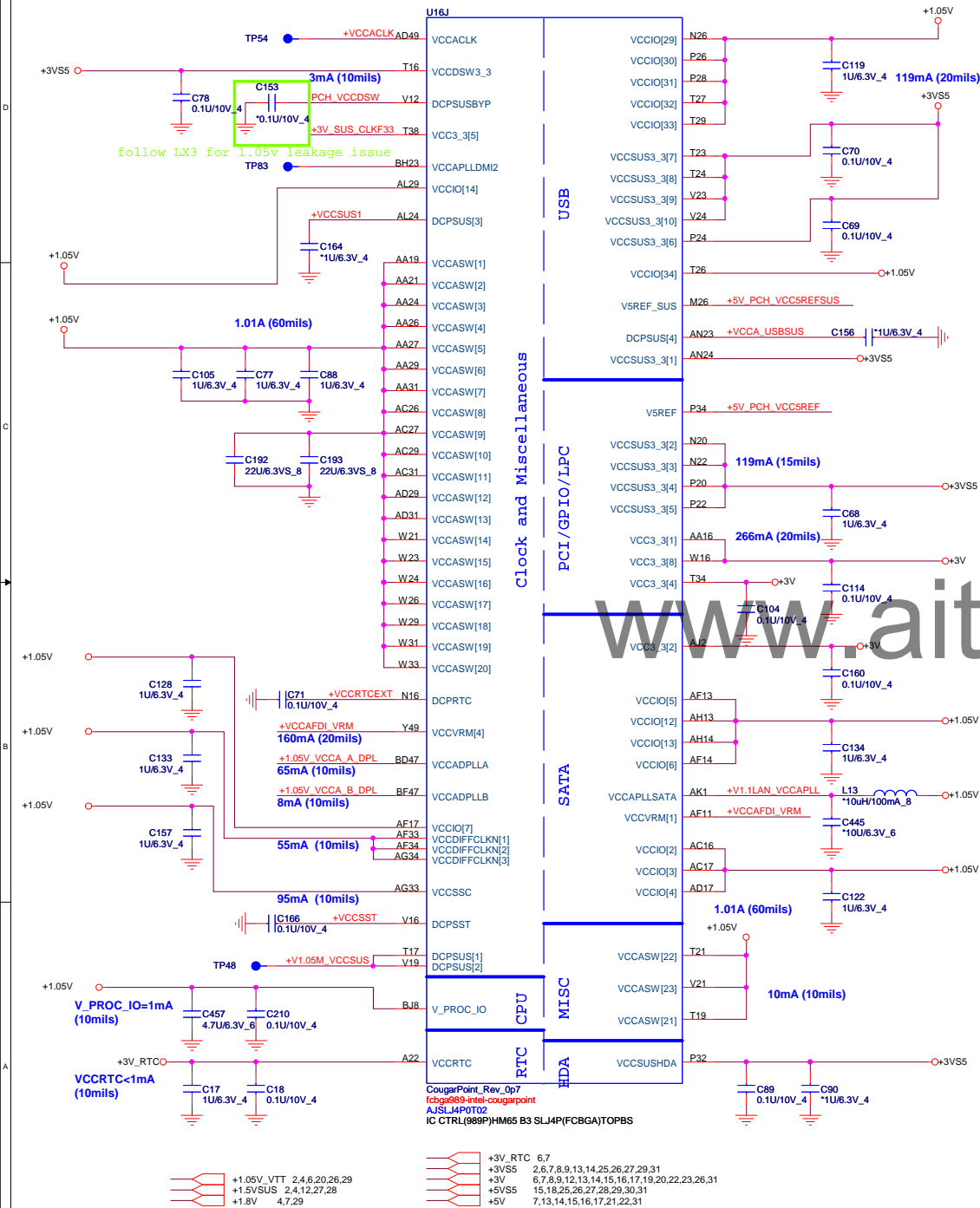
BOARD ID SETTING

BOARD ID SETTING	BOARD_ID0 GPIO 44	BOARD_ID1 GPIO 45	BOARD_ID2 GPIO 46
HR	0	0	0

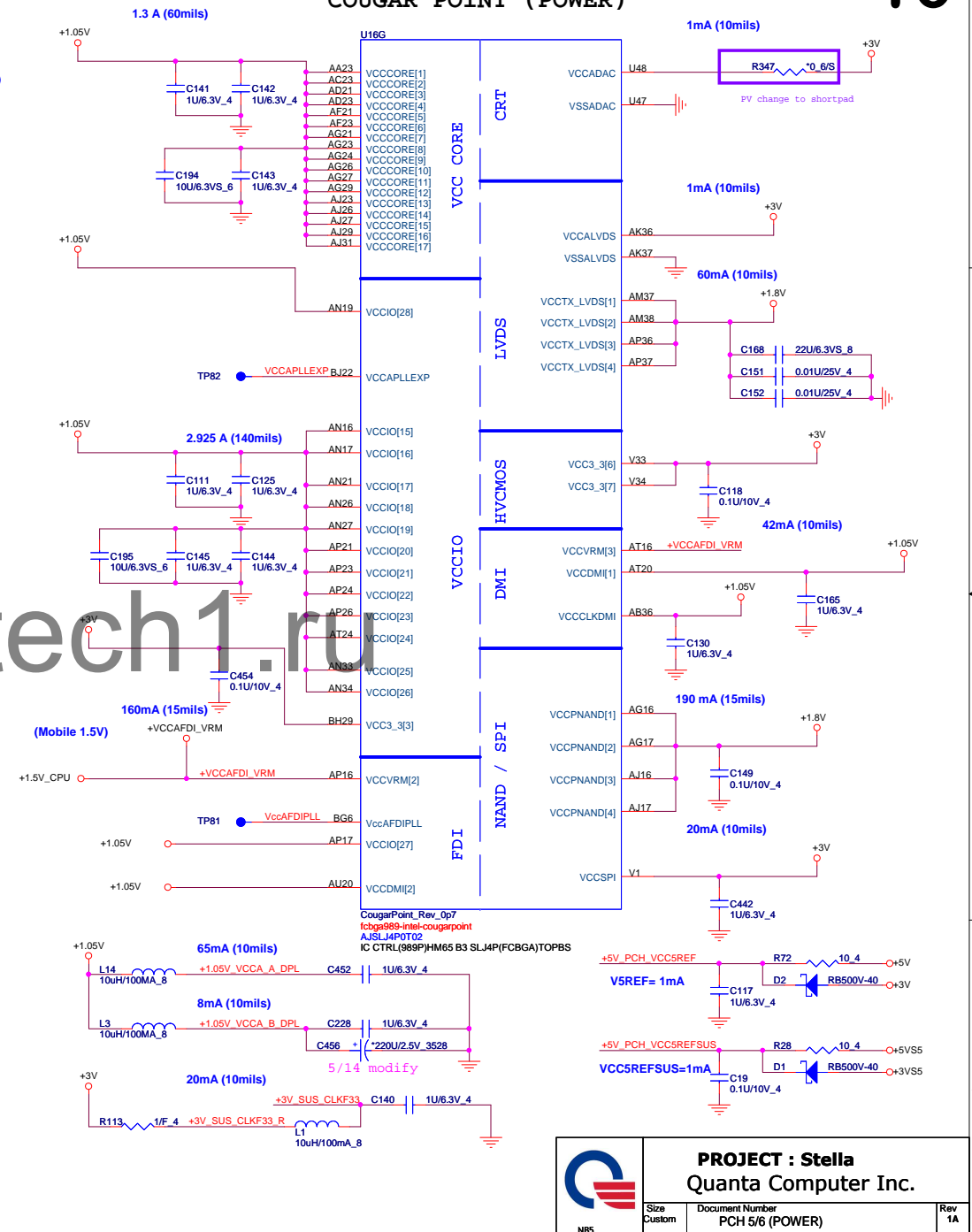
8 BOARD_ID0 BOARD_ID0 GPIO 44
8 BOARD_ID1 BOARD_ID1 GPIO 45
8 BOARD_ID2 BOARD_ID2 GPIO 45



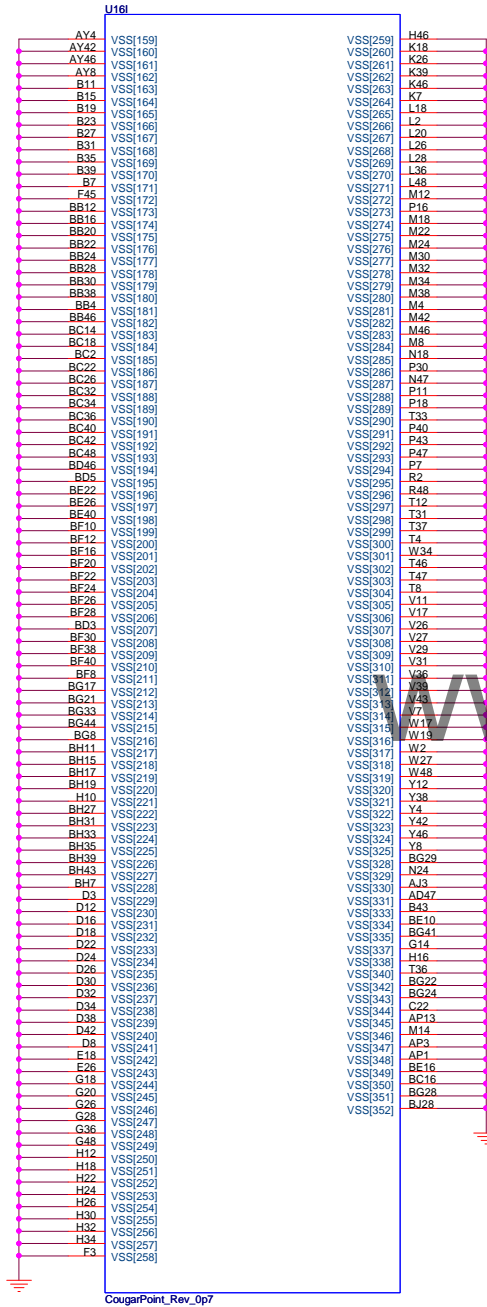
Cougar Point-M (POWER)



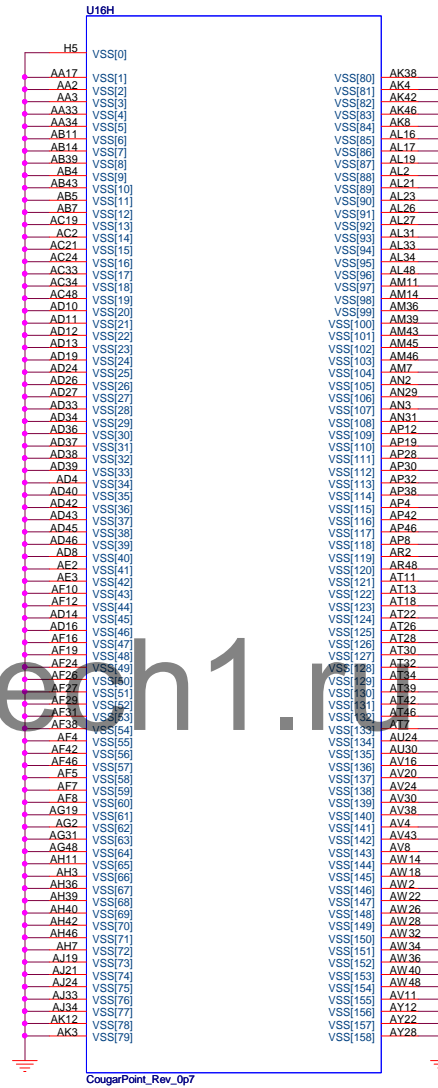
COUGAR POINT (POWER)

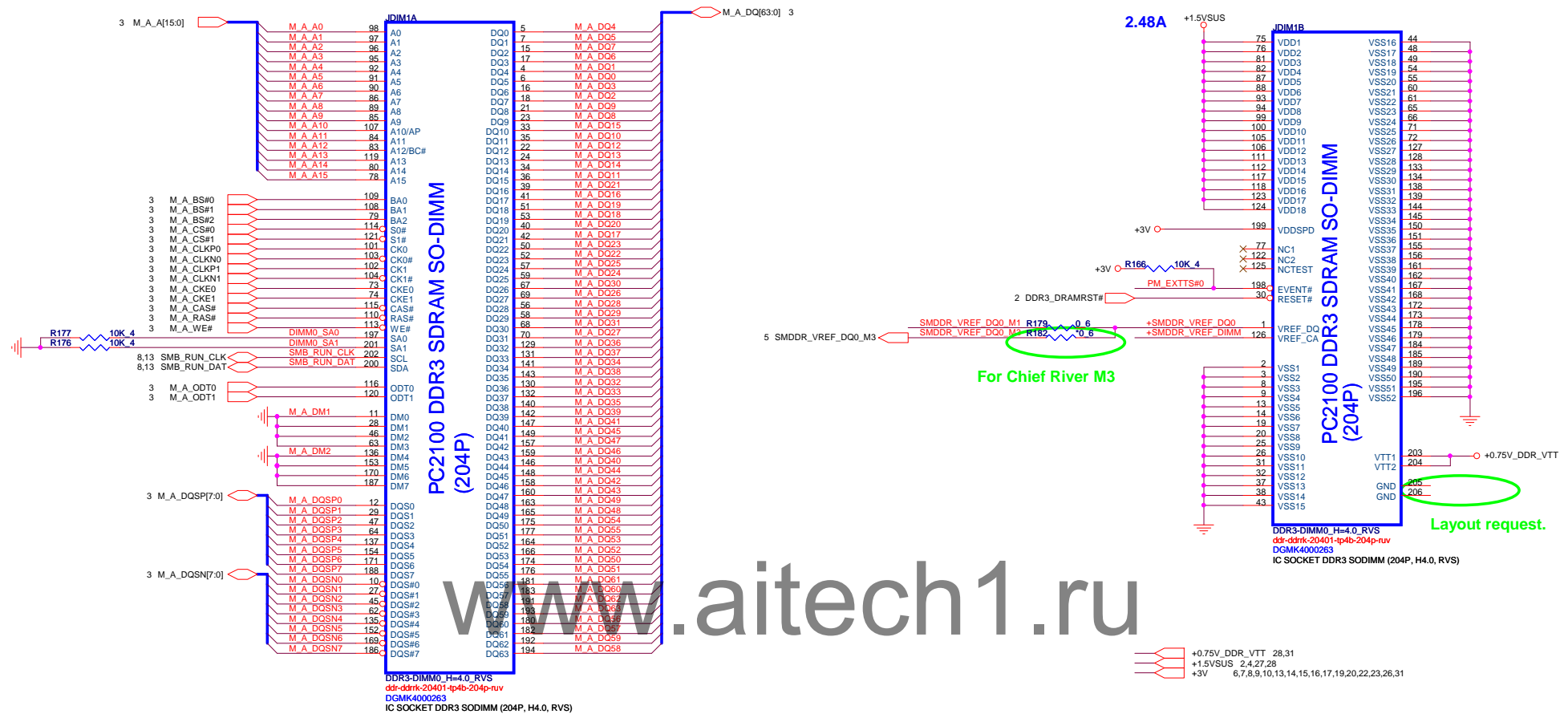


IBEX PEAK-M (GND)



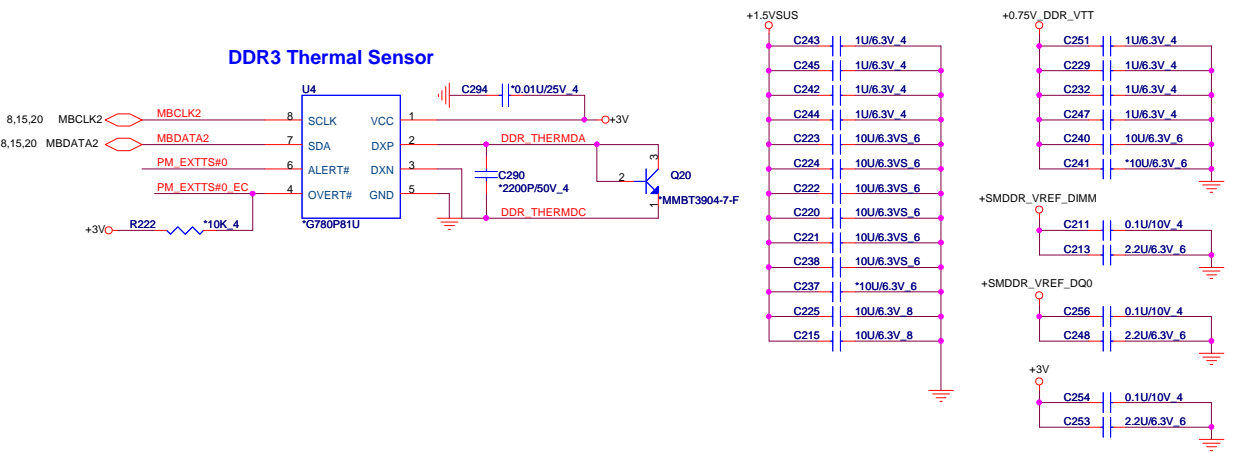
IBEX PEAK-M (GND)



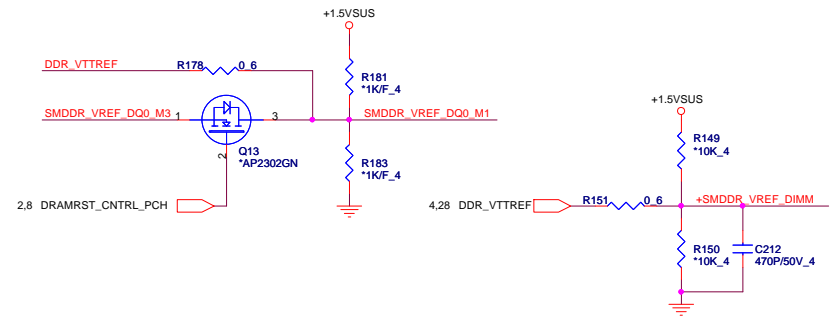


www.aitech1.ru

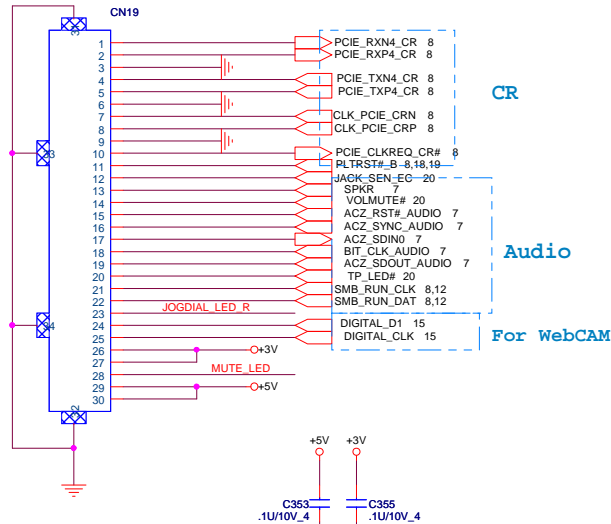
Place these Caps near So-Dimm0.



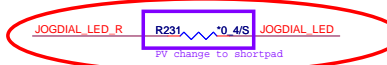
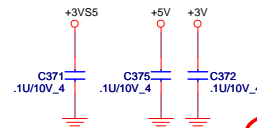
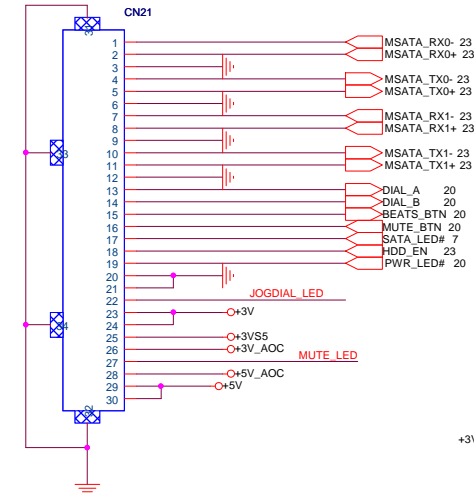
VREF DQ0 M1 Solution



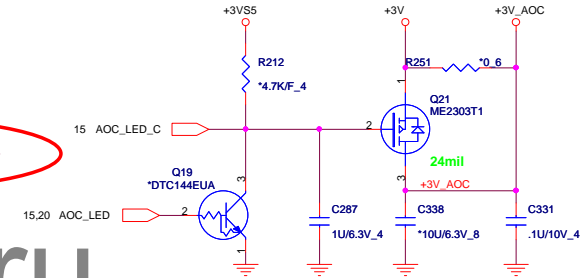
FOR AUDIO/CR



FOR mSATA

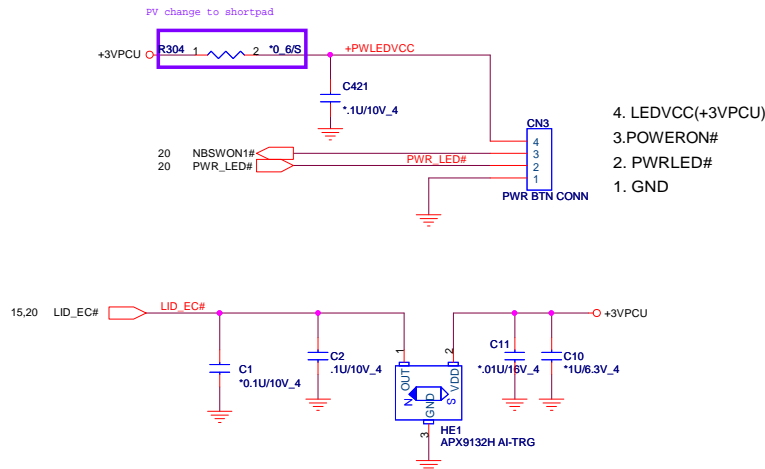


SI add



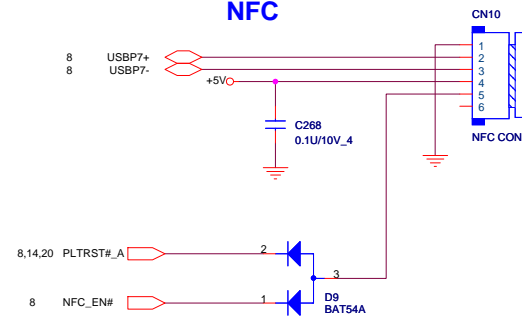
www.aitech1.ru

POWER BUTTON

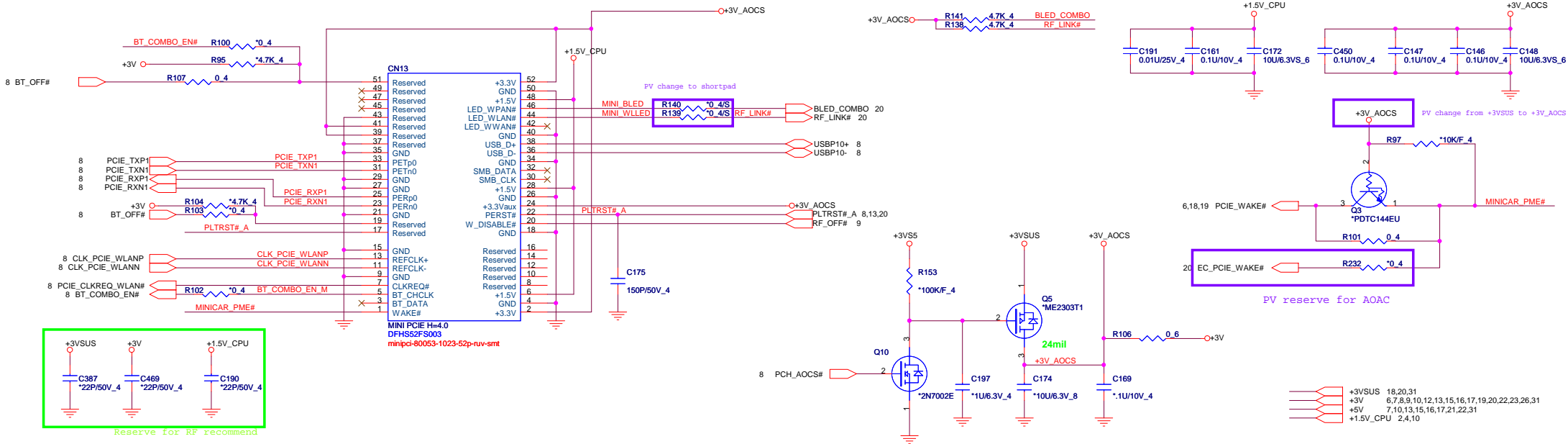
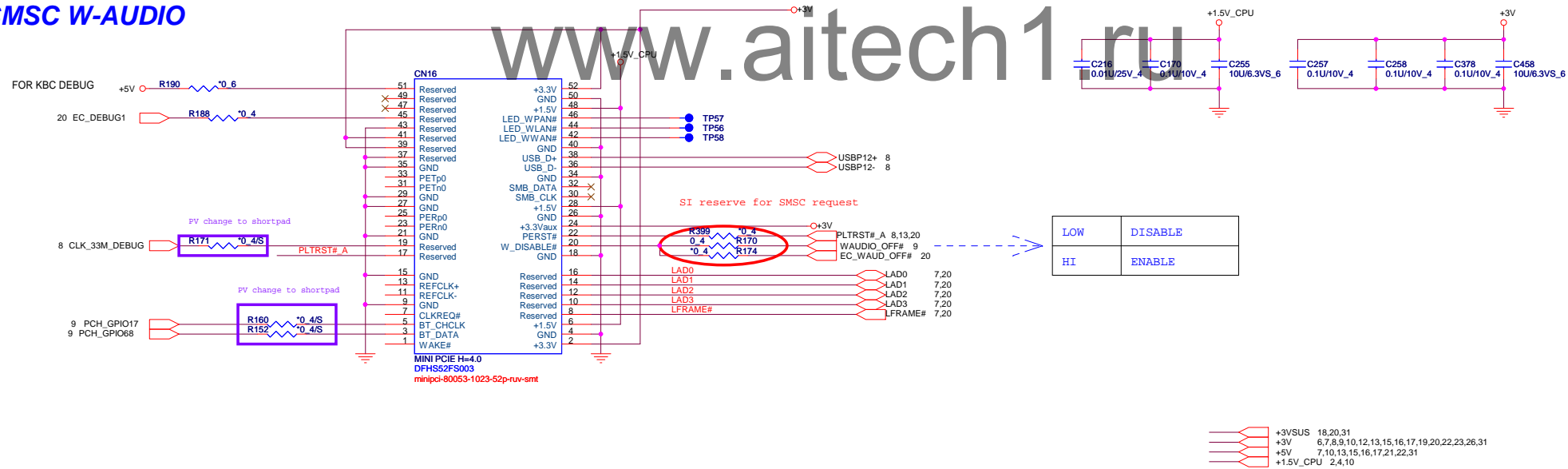


1. GND
2. PWRLED#
3. POWERON#
4. LEDVCC(+3VPCU)

NFC

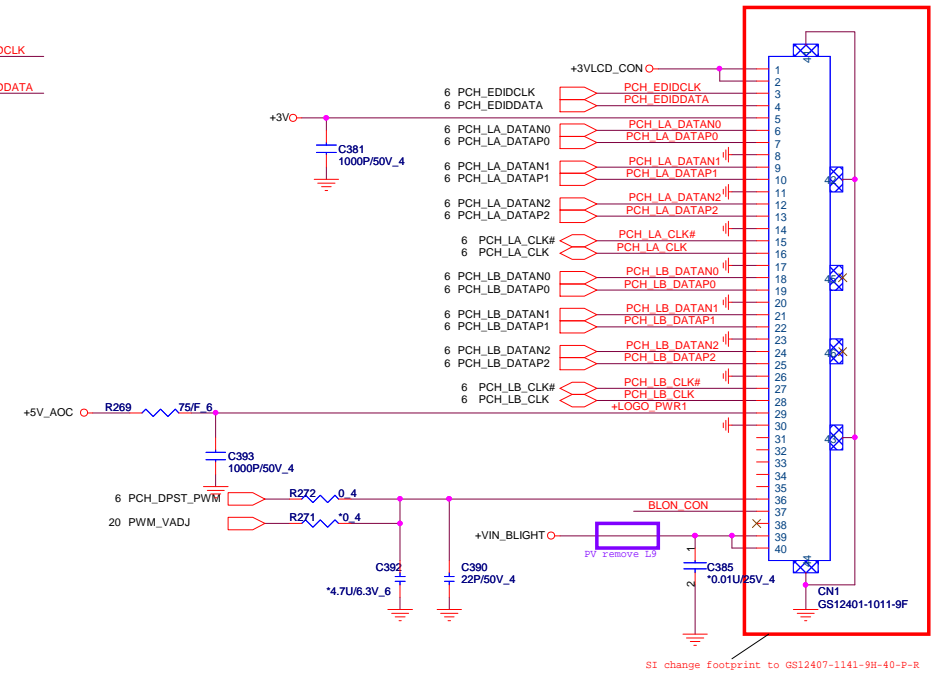
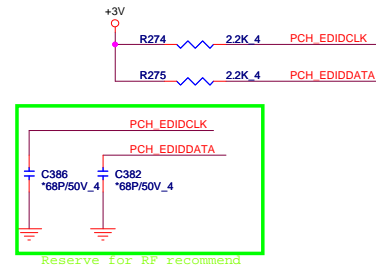
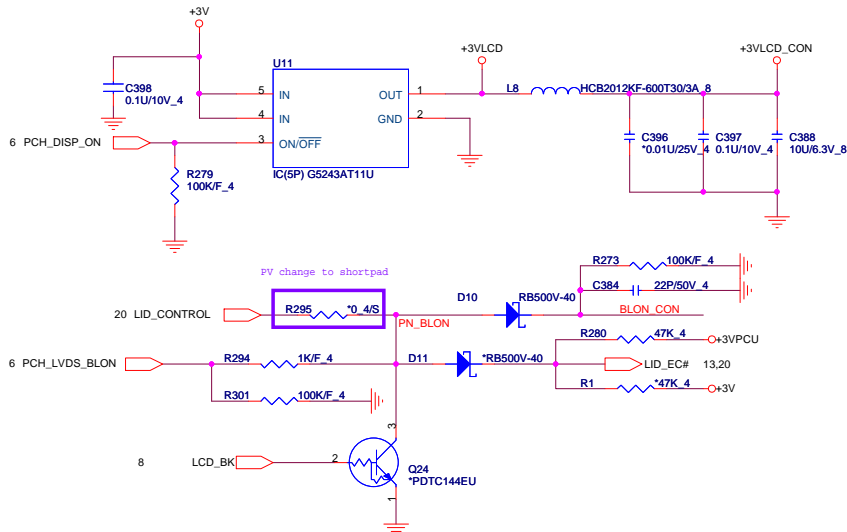


Mini PCI-E Card 1 WLAN+BT

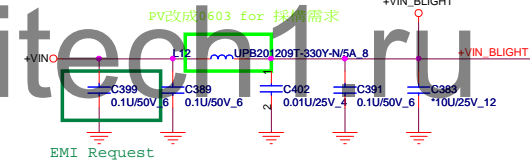
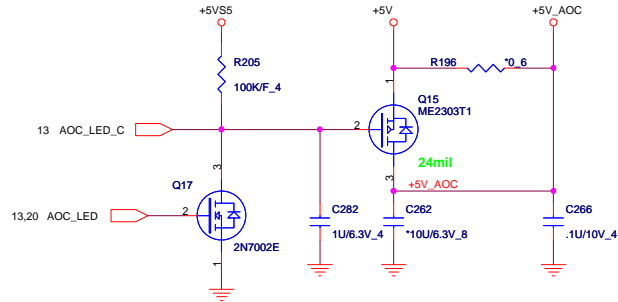
**Mini PCI-E Card 1**
SMSC W-AUDIO

PROJECT : Stella
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN	Rev 1A
Date: Friday, September 09, 2011		Sheet 14 of 31

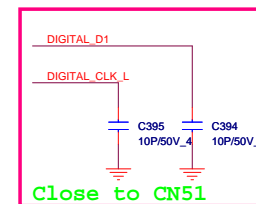
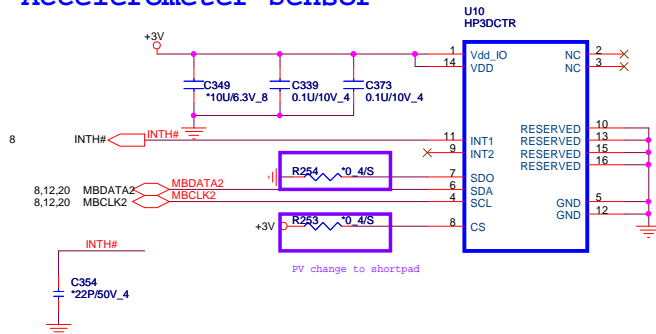


Support AOC function

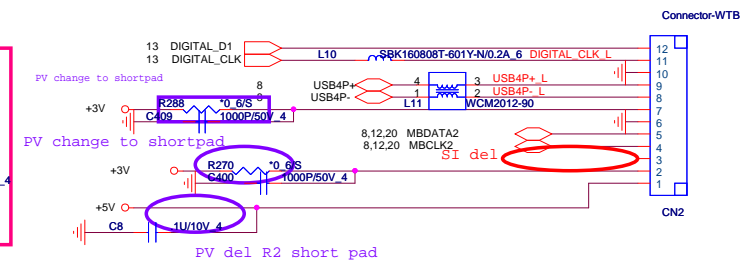


SGT-HP3DCTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

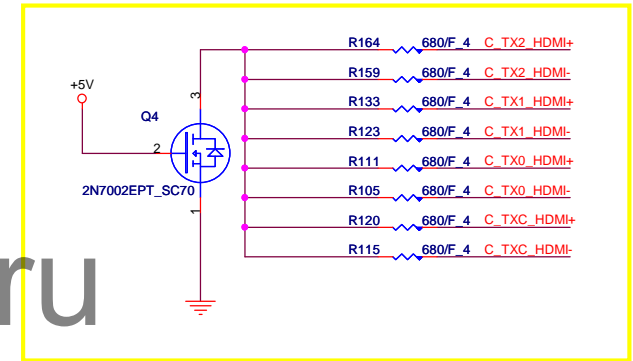
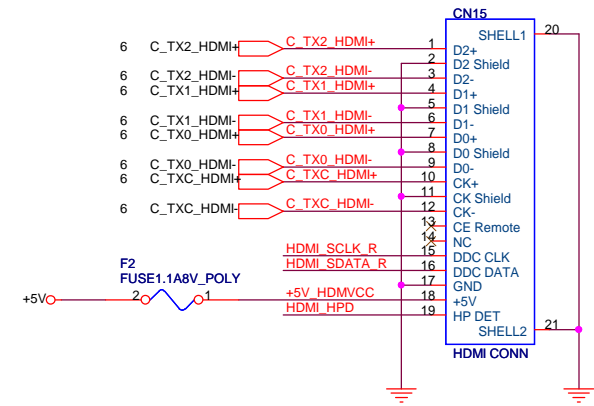
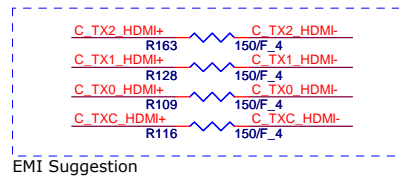
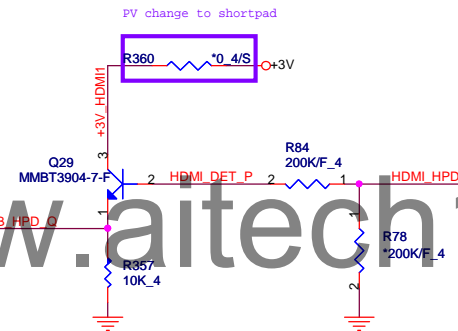
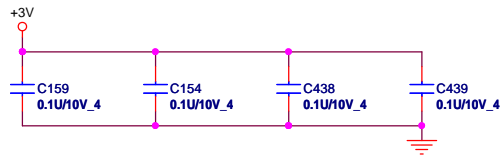
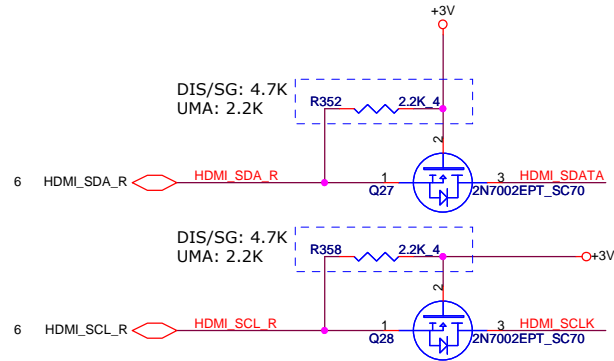
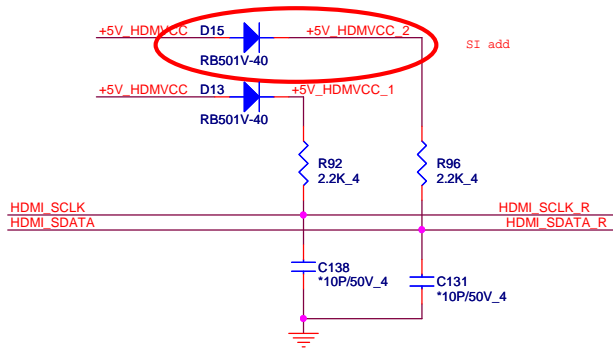
Accelerometer Sensor



WebCam/LDPS CONNECTOR

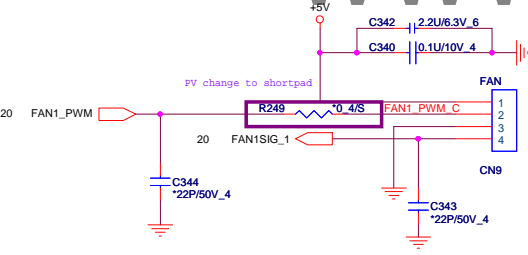


HDMI CON_COM

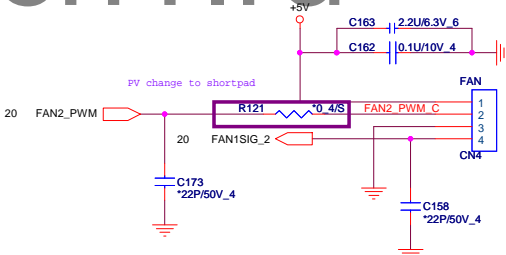


7,10,13,14,15,16,21,22,31 +5V
6,7,8,9,10,12,13,14,15,16,19,20,22,23,26,31 +3V

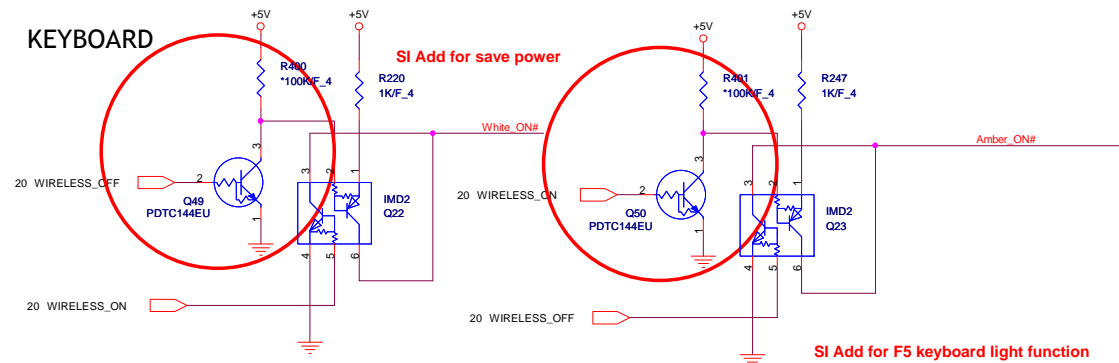
CPU FAN1



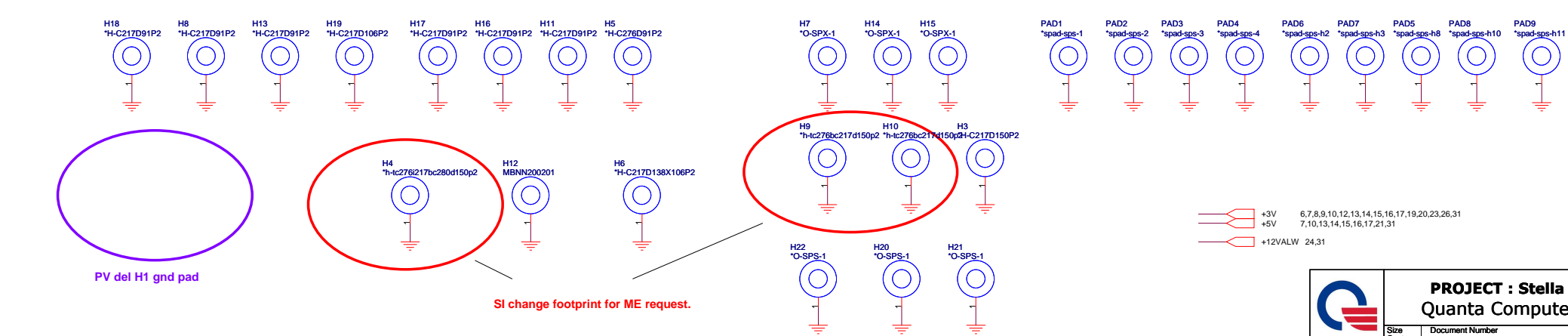
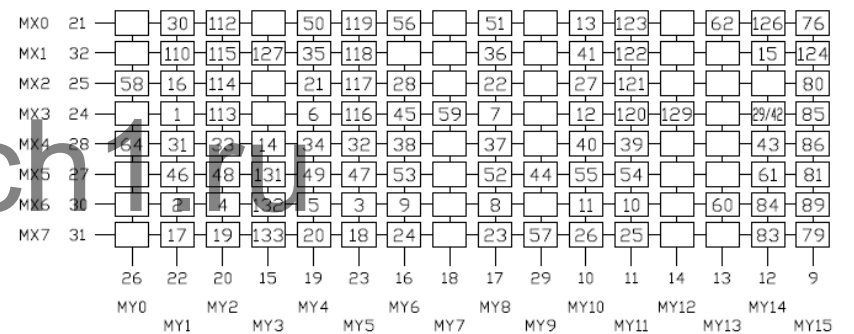
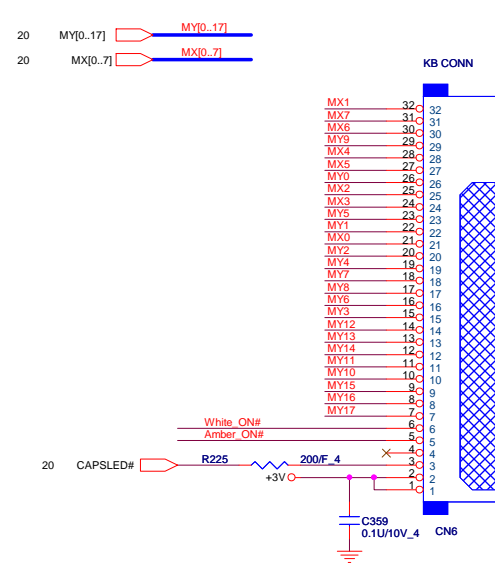
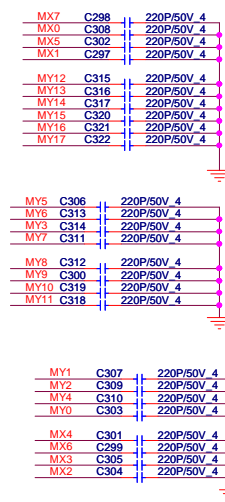
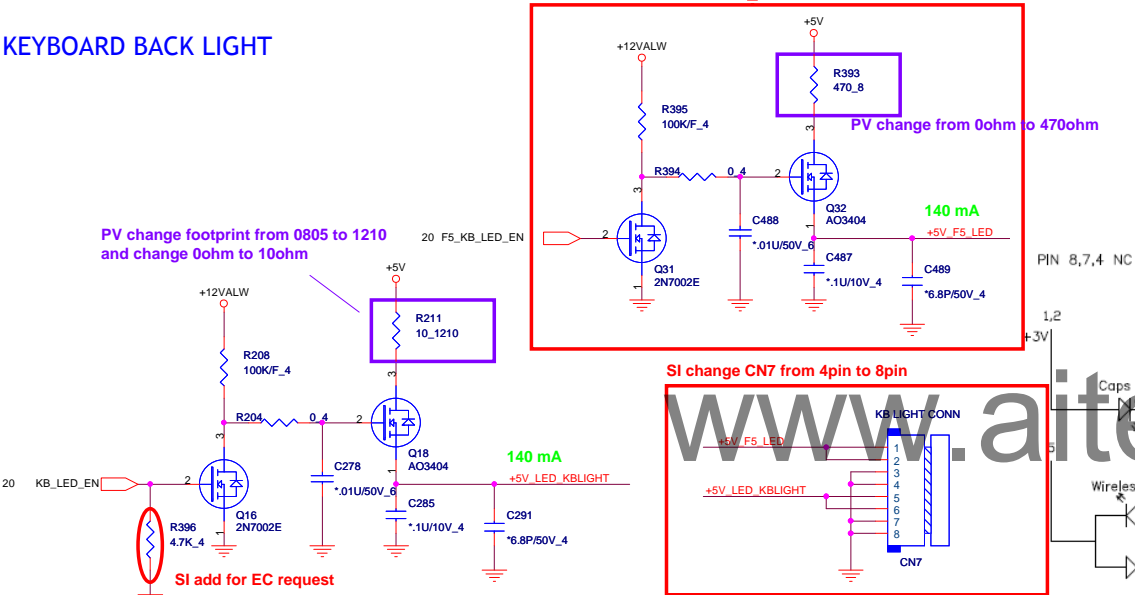
CPU FAN2



KEYBOARD

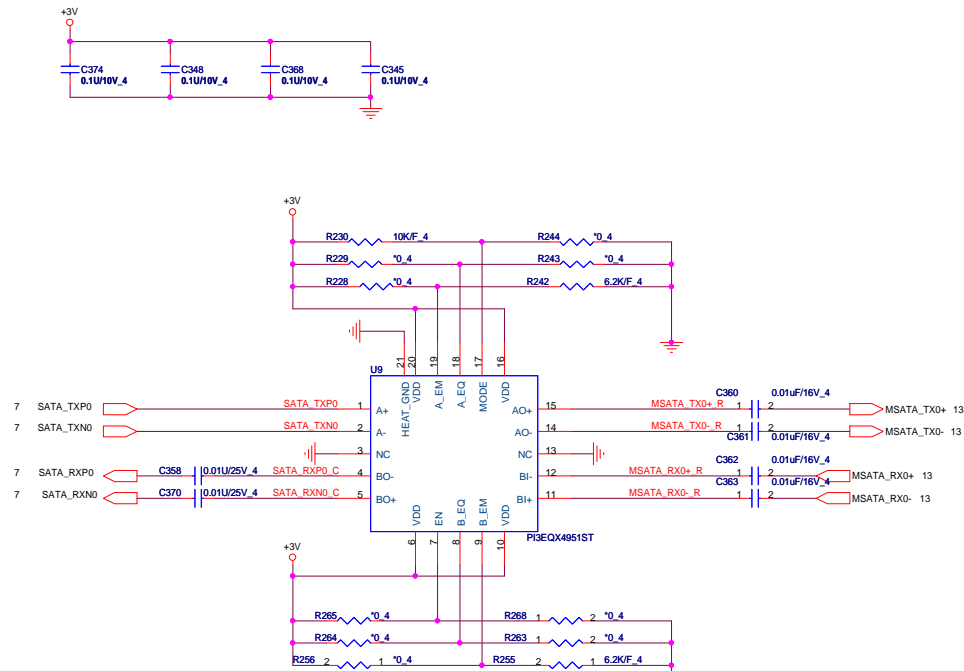


KEYBOARD BACK LIGHT

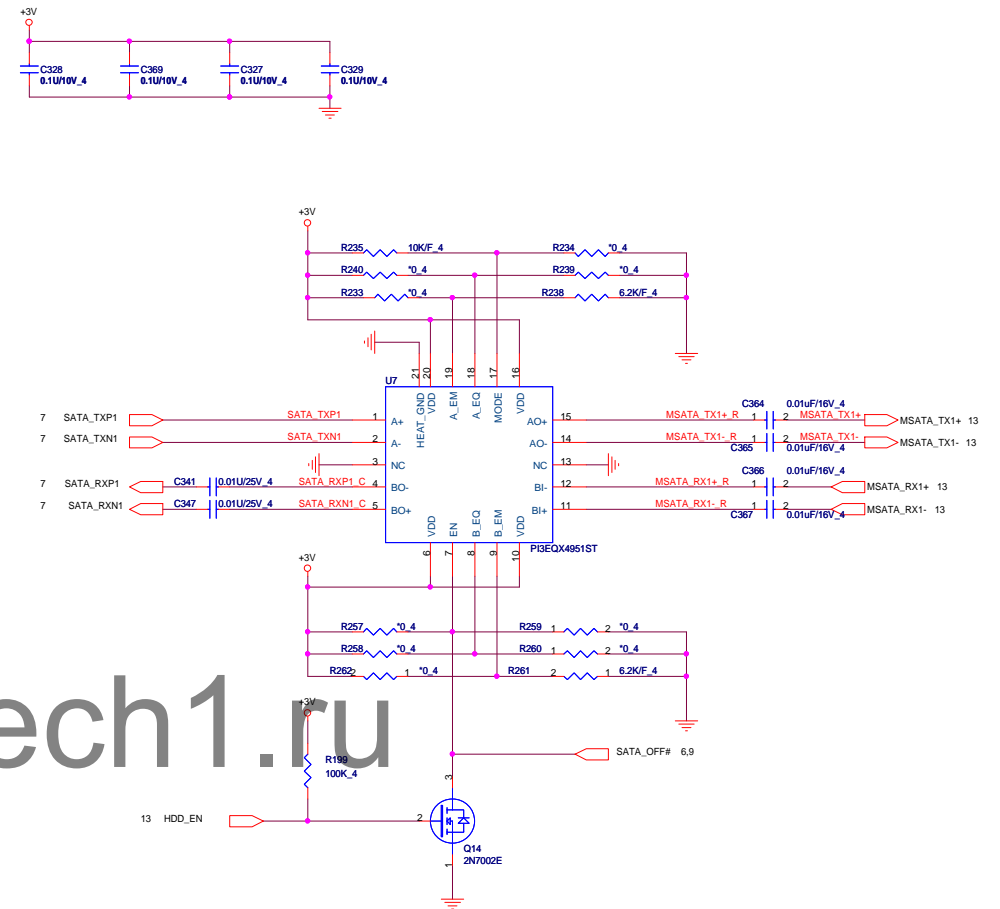


+3V 6,7,8,9,10,12,13,14,15,16,17,19,20,23,26,31
+5V 7,10,13,14,15,16,17,21,31
+12VALW 24,31

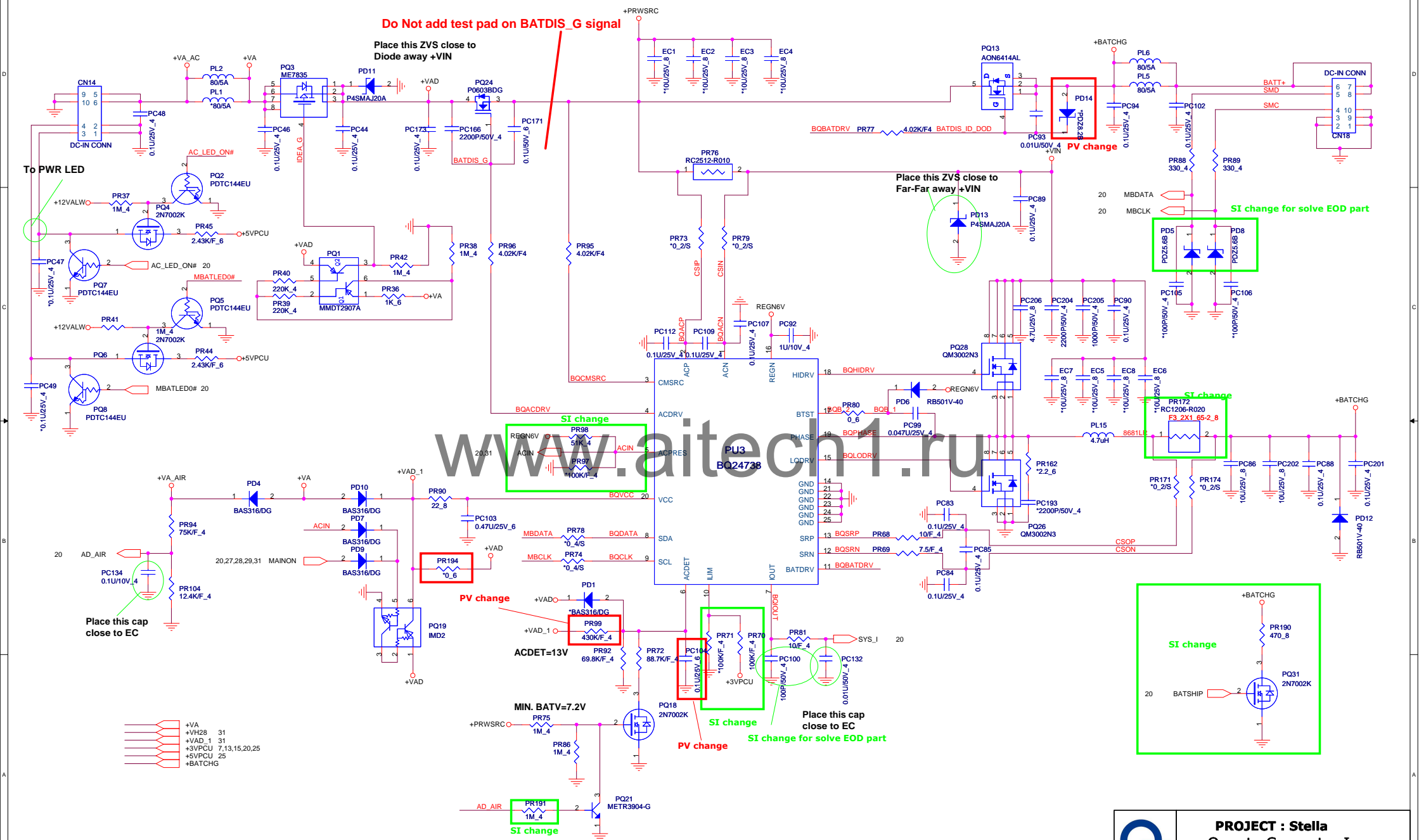
HDD0 mSATA 1ST

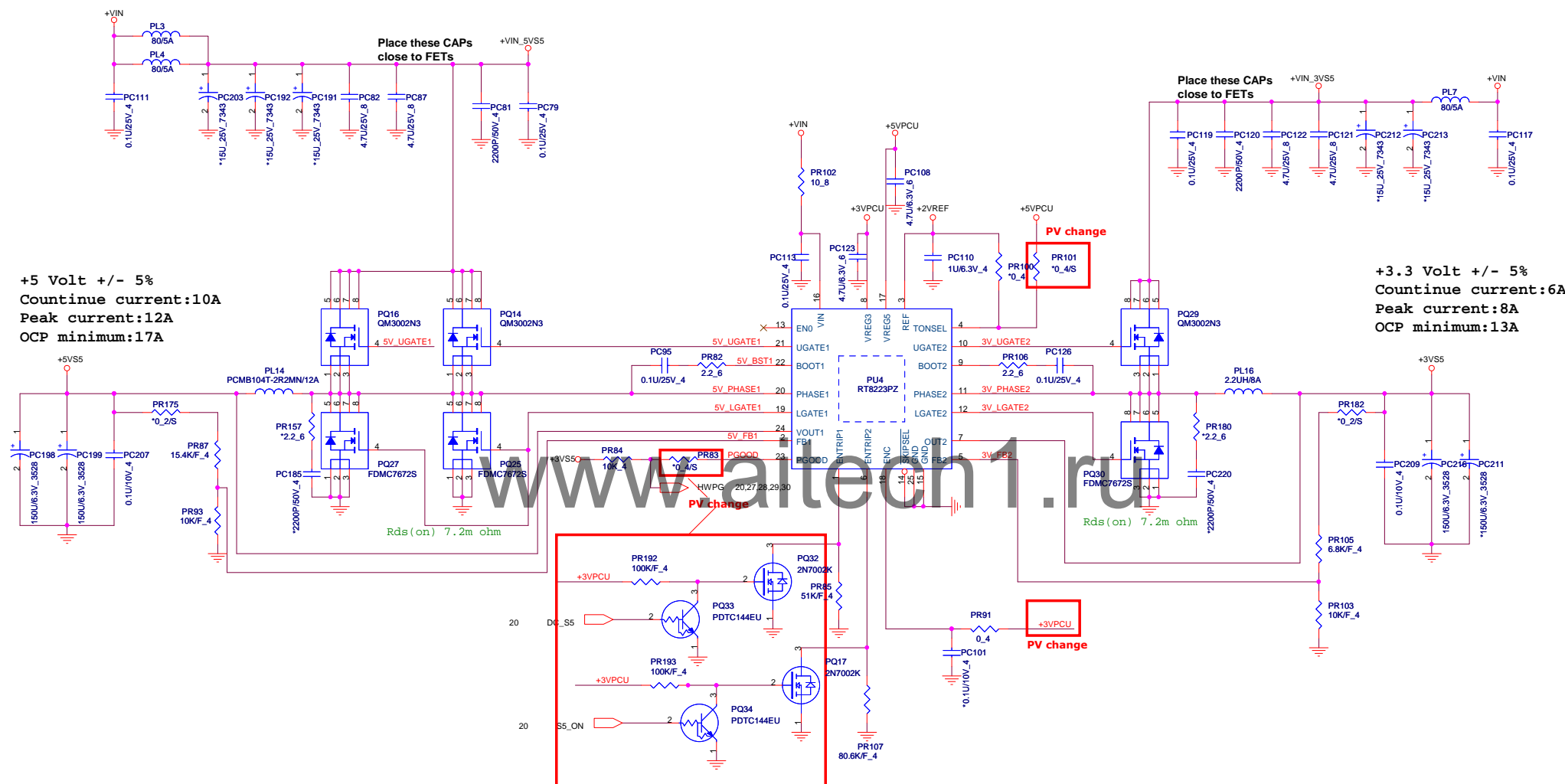


HDD1 mSATA 2ND

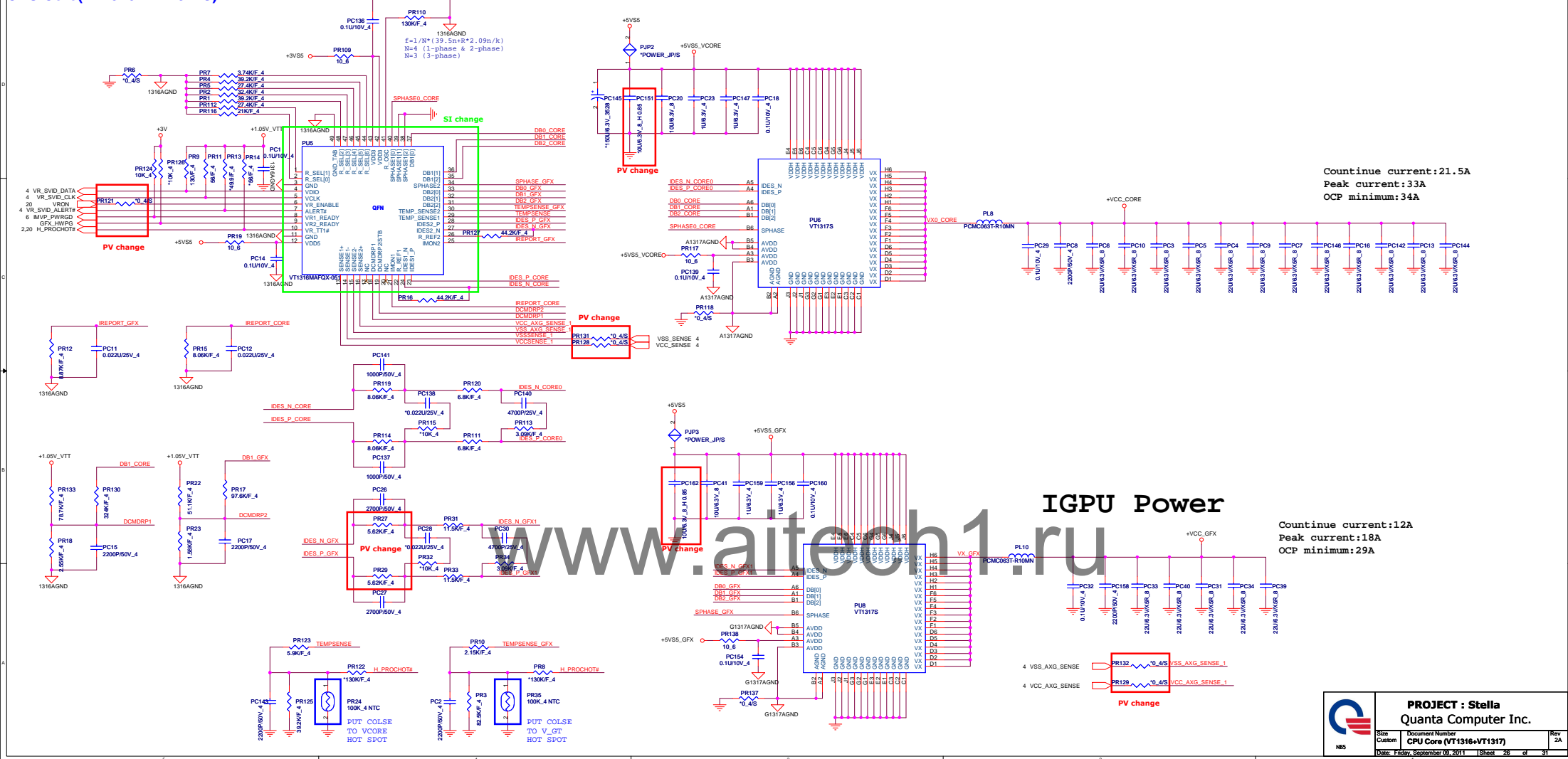


www.aitech1.ru

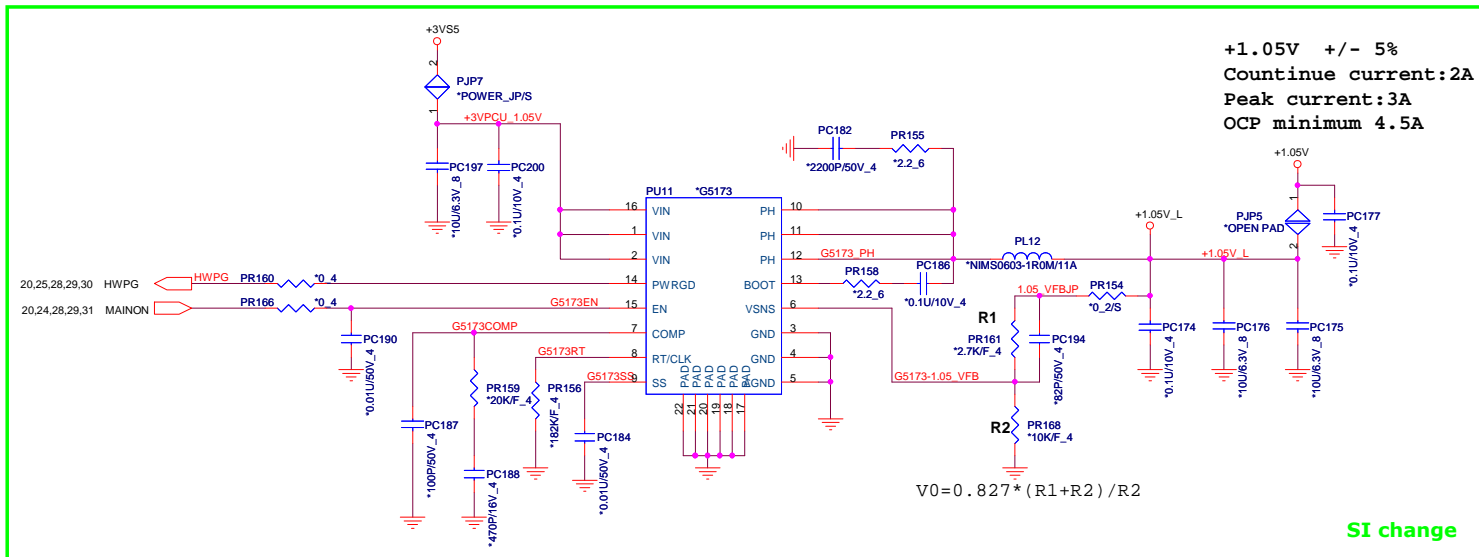




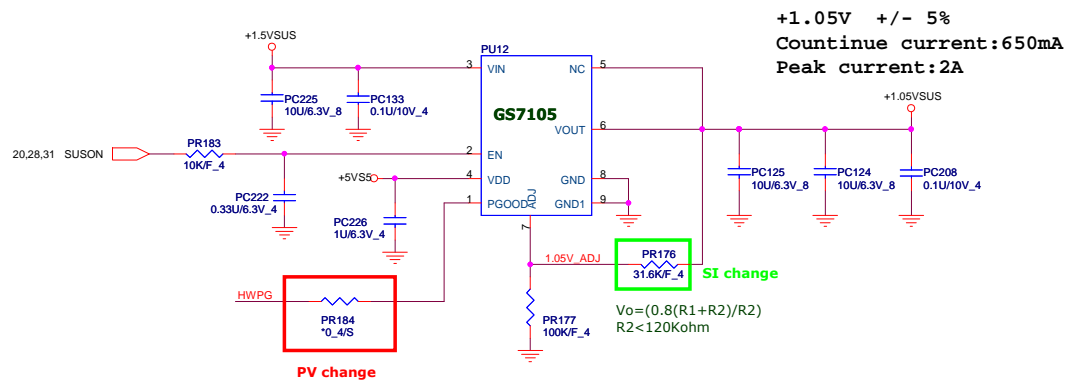
CPU Core(VT1316M+VT317S)



VCCP1.05V

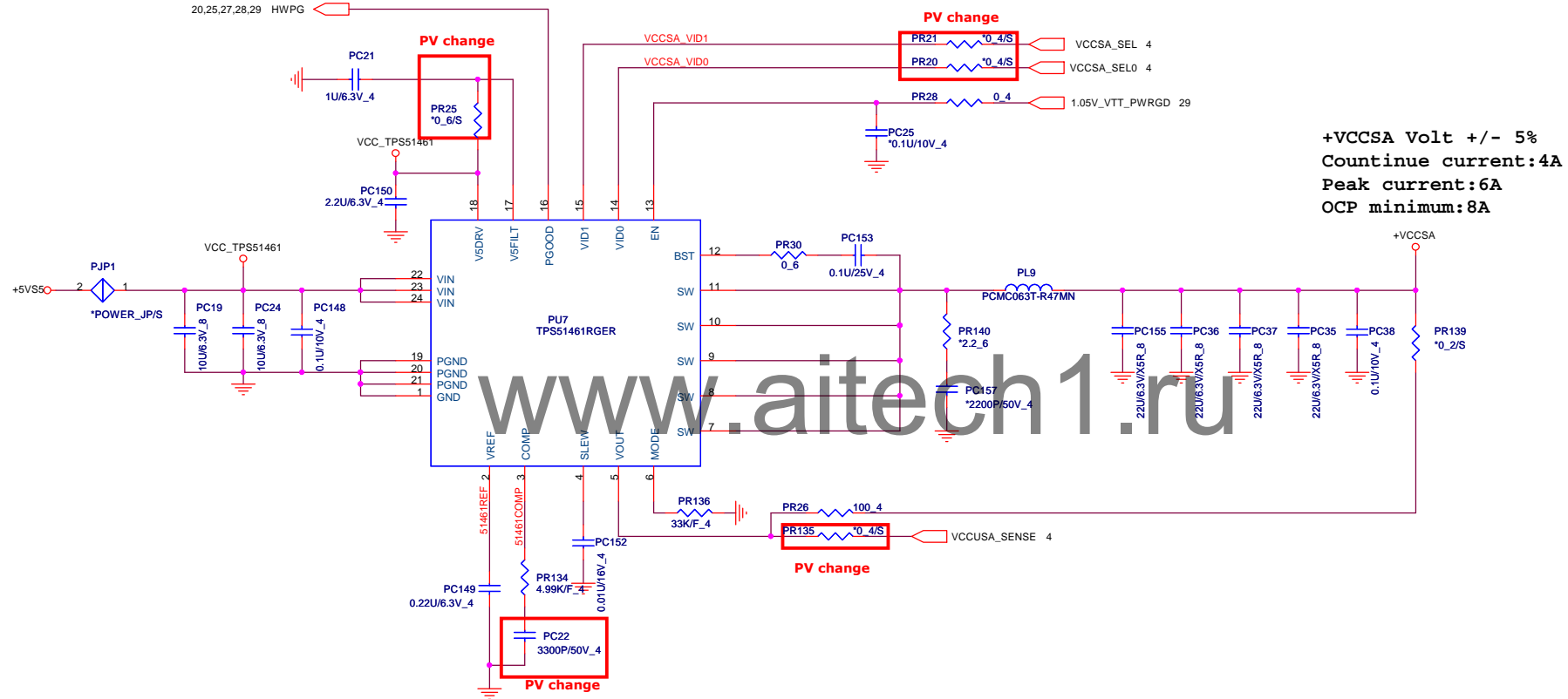


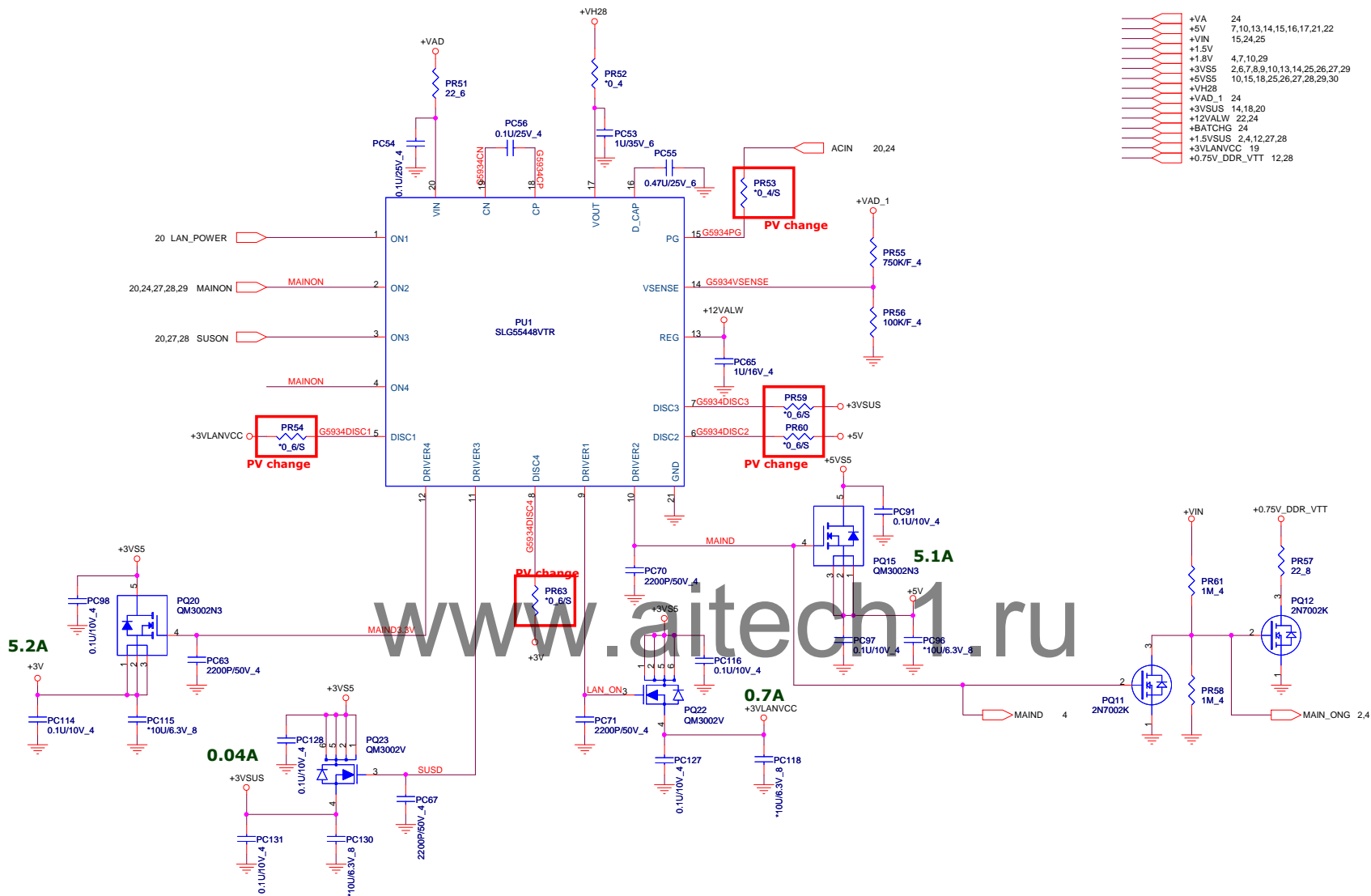
www.aitech1.ru



CPU system agent
voltage slew rate of 0.5 -10 mV/μs

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V





+VA	24
+5V	7,10,13,14,15,16,17,21,22
+VIN	15,24,25
+1.5V	
+1.8V	4,7,10,29
+3VS5	2,6,7,8,9,10,13,14,25,26,27,29
+5VS5	10,15,18,25,26,27,28,29,30
+VH28	
+VAD_1	24
+3VSUS	14,18,20
+12VALW	22,24
+BATCHG	24
+1.5VSUS	2,4,12,27,28
+3VLAVCC	19
+0.75V_DDR_VTT	12,28